TITLE OF THE INVENTION

Communication System Using Digital Watermark for Synchronising Multiplexed Text Data to Video Frames

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to video communication systems and more specifically to a copy-protect video communication system. The present invention is particularly useful for standard digital television broadcasting.

Description of the Related Art

For standard digital television broadcasting, it is contemplated to multiplex text data with a video signal using vertical blanking intervals. For this purpose, a number of text data are multiplexed in a video program and each text data stream is associated with a particular series of video frames, or "events" so that each text appears on the screen of television receivers simultaneously with the associated event. In order for television receivers to synchronise a text data stream with the associated event, it is necessary for the broadcasting station to transmit timing information along with a video signal, as disclosed in Japanese Laid-Open Patent Application 11-27641. However, the use of timing information represents a waste of resource of the video frequency spectrum.

On the other hand, digital (or electronic) watermark is currently receiving attention because of its ability to detect illegal duplication of video programs and a number of techniques have been developed for

hiding (embedding) identifying information into programs to be copy-protected.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a system and method for synchronising text data streams to "events" of digital video stream without using timing information.

The stated object is obtained by embedding a digital watermark in the transmitted video stream and detecting the digital watermark in the received video stream and using it as a timing signal for synchronising a text data stream to associated video frames.

According to one aspect of the present invention, there is provided a digital video communication system comprising, at a source site, an embedding circuit for embedding a digital watermark in a digital video stream to produce a watermarked digital video stream, and a multiplexer for multiplexing a text data stream with the watermarked digital video stream to produce a multiplexed signal. At a sink site, the system includes a demultiplexer for demultiplexing the multiplexed signal for recovering a watermarked digital video stream and a text data stream. A digital watermark detector is provided for detecting the digital watermark embedded in the recovered digital video stream. A synchroniser responds to the detected digital watermark for synchronising the recovered text data stream to the recovered video stream.

According to a second aspect, the present invention provides a digital video communication method comprising the steps of embedding

a digital watermark in a digital video stream to produce a watermarked digital video stream, multiplexing a text data stream with the watermarked digital video stream to produce a multiplexed signal, demultiplexing the multiplexed signal for recovering a watermarked digital video stream and a text data stream, detecting the digital watermark embedded in the recovered digital video stream and using the detected digital watermark as a timing signal for reading the text data from said storage medium, and synchronising the recovered text data stream with the recovered digital video stream in response to the detected digital watermark.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a digital video communication system according to the present invention;

Fig. 2 is a timing diagram of a video stream along with text data which occur at such timing that write and read operations can be performed in an alternate fashion;

Fig. 3 is a timing diagram of a video stream along with text data which occur at such timing that write and read operations are performed simultaneously by using a dual-mode memory;

Fig. 4 is a block diagram of a first modified embodiment of the present invention;

Fig. 5 is a block diagram of a second modified embodiment of the present invention;

Fig. 6 is a timing diagram of a video stream along with text data which occur at such timing that write and read operations are performed simultaneously for different text data by using switched memories; and

Fig. 7 is a block diagram of a third modified embodiment of the present invention associated with Fig. 6.

DETAILED DESCRIPTION

In Fig. 1, a video communication system according to one embodiment of the present invention is comprised by a transmitter 10 which transmits a composite digital video signal through a noisy environment such as a cable or a wireless transmission system (including satellite and terrestrial broadcasting) or a storage system such as video cassette recorder 20 to a receiver 30.

At the transmitter 10, a digital audio stream is processed by an audio compression circuit 11 and a textual data stream is processed by a data compression circuit 12. A digital video stream is combined with a watermark signal in an embedding circuit 13 so that the watermark is embedded in a series of video images. A suitable method for the digital watermark is described in Japanese Laid-Open Patent Application 10-155151. The output of embedding circuit 13 is processed by a video compression circuit 14 using a known compression technique such as MPEG-2 to produce an MPEG-2 transport video stream.

The outputs of the audio and data compression circuits 11 and 12 are multiplexed with the MPEG-2 transport video stream by a multiplexer 15 to produce a composite video signal by inserting the textual data into the vertical blanking intervals of the video format and

the audio signal into the low frequency region of the spectrum of the composite video signal.

The output of multiplexer 15 is encrypted by an encryption circuit, or encryptor 16. A forward error correction (FEC) encoder 17 is provided for converting the output of the encryptor 16 into a format that allows errors in the transmitted signal to be detected and corrected at the intended receive site. The output of the FEC encoder 17 is converted by an interface 18 to a radio frequency signal and transmitted to the receiver 30 if the intermediate system 20 is a transmission system. If the system 20 is a storage system, the output of the FEC encoder 17 is directly supplied to the storage system and stored in a suitable storage medium.

The signal from the transmitter 10 is received by an interface 31 at the receiver 30 to produce a replica of the output signal of the FEC encoder 17. If the intermediate system 20 is a wireless link, the received signal is down-converted by the interface 31 to the baseband signal and if it is a storage system the stored signal is a baseband signal.

The received baseband signal is applied to an FEC decoder 32 where errors, if present in the received signal, are detected and corrected. The error-corrected signal is decrypted by a decryptor 33 and fed to a demultiplexer 34 to decompose the decrypted signal into the compressed audio, data and MPEG-2 transport video components, which are expanded to the original format by respective expansion circuits 35, 36 and 37.

The text data recovered by data expansion circuit 36 is supplied to a memory or synchroniser 37 and the MPEG-2 transport video stream

recovered by the video expansion circuit 38 is supplied to a watermark detector 39 to detect the watermark embedded in the video stream in a manner as disclosed in the aforesaid Japanese laid-open patent application.

The detected watermark signal is used by the memory 37 as a read timing signal for reading the stored text data so that it is synchronised to a series of desired video frames. The detected watermark is also supplied to a copy protect circuit 40 to produce a copy management signal that is used to protect video programs from being illegally copied by unauthorised users. The copy management signal is embedded in the video stream from video expansion circuit 38 as a digital watermark by an embedding circuit 41 to protect a series of video frames from unauthorised duplications.

The text data from the memory 37 and the output of embedding circuit 41 are supplied to a video display system 42.

An example video stream is shown in Fig. 2 in which multiplexed text data 1 and 2 occur at such timing that the memory 37 can operate alternately in a write mode and a read mode. Two watermark signals are shown embedded in a video stream for synchronising text data 1 to a series of video frames 1 to 4 (event 1), and synchronising text data 2 to a series of video frames 5 to 8 (event 2). When the video stream is displayed on the display system 42, the event-1 video frames 1 to 4 will be overlaid with text data 1 and the event-2 video frames 5 to 8 will be overlaid with text data 2.

Preferably, the memory 37 is of a dual-mode type in which it

operates simultaneously in write and read modes. As shown in Fig. 3, this mode of operation is useful when a read operation of text data 1 and 2 is started while they are still written into the memory.

In a modified embodiment shown in Fig. 4, a video overlay unit 43 is provided between the video expansion circuit 38 and the watermark embedding circuit 41. Video overlay unit 43 receives the output of memory 37 to superimpose the text data on video frames specified by the detected digital watermark.

In a further modified embodiment shown in Fig. 5, the copy protect circuit 40 is replaced with a watermark converter 44 in which the watermark signal detected by the watermark detector 39 is altered into a form that can be detected as a copy management signal to protect specified video frames from being illegally copied by unauthorised users. The output of watermark converter 44 is combined with the output of video overlay unit 43 in the embedding circuit 41.

If text data 1 and 2 occur in sequence but the read timing of text data 1 coincides with the write timing of text data 2 as shown in Fig. 6, a modification of Fig. 7 is useful. In this modification, two graphic memories 61 and 62 are provided and a write control switch 63 is connected between the output of data expansion circuit 36 and the memories 61, 62 and a read control switch 64 is connected between the memories 61, 62 and the video overlay circuit 43. Memory control switches 63 and 64 are controlled by the output of the watermark detector 39 so that when one of the memories 61, 62 is in a write mode the other memory is in a read mode.